Q.P. Code: 19EC0409 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY: PUTTUR

(AUTONOMOUS)

B. Tech II Year II Semester Regular Examinations July-2021

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering**)**

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Discuss DC and AC characteristics of an ideal OP-AMP with relevant expressions.	L2	**6M**
	b	Explain the operation of an Instrumentation amplifier with neat sketch.	L3	**6M**
		OR		
2	**a**	Discuss differential amplifier with differential mode & common mode gain expressions.	L3	**6M**
	b	Discuss about Schmitt trigger with neat sketches.	L3	**6M**

UNIT-II

3	**a**	Explain and derive the time period for Astable multivibrator using 555 timer.	L2	**6M**
	b	Design Wien bridge oscillator using op-amp and explain its operation.	L4	**6M**
		OR		
4	**a**	Design and explain narrow band pass filter and discuss its frequency responses.	L4	**6M**
	b	Explain how 555 timer can be used as Monostable multivibrator with time period.	L2	**6M**

UNIT-III

5	**a**	Draw and Explain about the block schematics of PLL.	L2	**6M**
	b	Draw and explain about R-2R DAC with pros and cons.	L3	**6M**
		OR		
6	**a**	Draw and Explain about the Basic IC Voltage Regulators.	L2	**6M**
	b	Draw the circuit diagram of basic CMOS gate and explain its operation.	L3	**6M**

UNIT-IV

7	**a**	Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c.d) Also draw the relevant logic diagram.	L6	**6M**
	b	Discuss about behavioral design element with an example.	L4	**6M**
		OR		
8	**a**	Explain in detail different modeling styles of VHDL with suitable examples.	L2	**6M**
	b	Design the logic circuit and write VHDL program for the following function. F(X) = Σ A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11).	L6	**6M**

UNIT-V

9	**a**	Draw logic symbol of 74 x 85, 4-bit comparator & write a VHDL code for it.	L3	**6M**
	b	Design a Full adder with Half adder's logic circuit.	L6	**6M**
		OR		
10	**a**	Write a VHDL code for a D-flip flop in behavioral model.	L2	**6M**
	b	Design an 8 -bit serial in and serial out shift register and write a VHDL code for it.	L6	**6M**

*** END ***